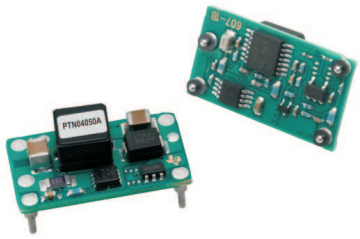
6-W, 3.3-V/5-V INPUT, WIDE ADJUST OUTPUT, POSITIVE-TO-NEGATIVE CONVERTER

FEATURES

- **Up to 6-W Output Power**
- **Wide-Input Voltage (2.9 V to 7 V)**
- **Wide-Output Voltage Adjust (–15 V to –3.3 V)**
- **High Efficiency (Up to 84%)**
- **On/Off Inhibit**
- **Output Current Limit**
- **Undervoltage Lockout**
- **Overtemperature Shutdown**
- **Operating Temperature: –40°C to 85°C**
- **Surface-Mount Package Available**

APPLICATIONS

- **General-Purpose, Industrial Controls, HVAC Systems, Test and Measurement, Medical Instrumentation, AC/DC Adaptors, Vehicles, Marine, and Avionics**

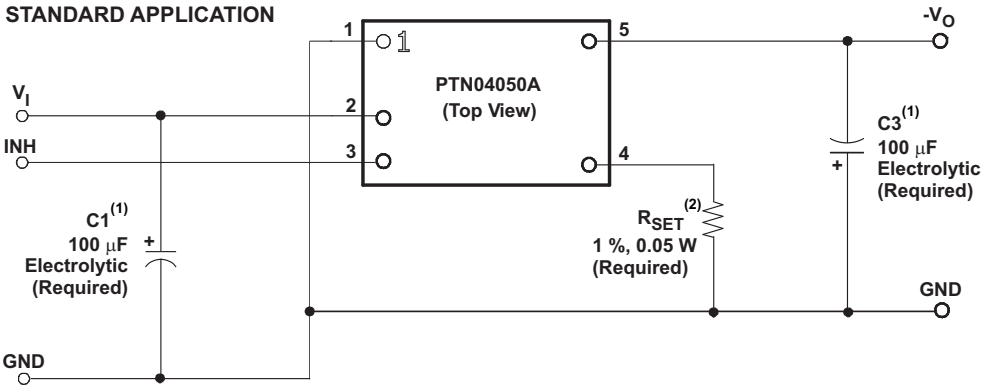


DESCRIPTION

The PTN04050A is an adjustable output, positive-to-negative, integrated switching regulator. In new designs, it should be considered in place of the PT5020 series of positive-to-negative integrated switching regulator products. The PTN04050A is smaller and lighter than its predecessor, with improved electrical performance characteristics, while operating over a wider input voltage range, with an adjustable output voltage. The caseless, double-sided package also exhibits improved thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range of 2.9 V to 7 V, the PTN04050A provides high-efficient, positive-to-negative voltage conversion for loads of up to 6 W. The output voltage is set using a single external resistor, and may be set to any value within the range, –15 V to –3.3 V.

The PTN04050A features include on/off inhibit, undervoltage lockout, over-current protection, and is suited for a wide variety of general-purpose applications that operate off 3.3-V or 5-V input.



(1) See the *Application Information* for capacitor recommendations.

(2) R_{SET} is required to adjust the output voltage. See the *Application Information* for values.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range unless otherwise noted
all voltages with respect to GND (pin 1),

			UNIT
T_A	Operating free-air temperature	Over V_I range	–40°C to 85°C
	Leaded temperature (H & D suffix)	20 seconds	260°C
	Solder reflow temperature (S suffix)	Surface temperature of module body or pins (20 sec)	235°C
	Solder reflow temperature (Z suffix)	Surface temperature of module body or pins (20 sec)	260°C (2)
T_{stg}	Storage temperature		–40°C to 125°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Moisture Sensitivity Level (MSL) rating Level-3-260C-168HR

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	Input voltage	2.9	7	V
T_A	Operating free-air temperature	–40	85	°C
P_O	Output power		6	W

PACKAGE SPECIFICATIONS

PTN04050A (Suffix AH, AD, AS and AZ)			
Weight			2.7 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, ½ sine, mounted		500 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH & AD)	20 G (1)
		Horizontal SMD (suffix AS & AZ)	15 G (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 5 V, V_O = –12 V, I_O = I_O (max), C_I = 100 µF, C_O = 100 µF (unless otherwise noted)

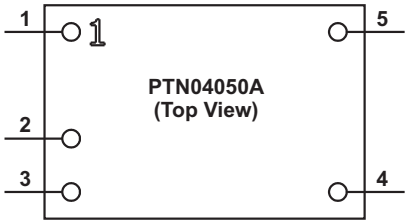
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 85°C, natural convection airflow	V_O = –3.3 V to –6 V	0.2 (1)		1.0 (2)	A
			V_O = –9 V	0.1 (1)		0.6 (2)	
			V_O = –12 V	0.1 (1)		0.5 (2)	
			V_O = –12.6 V to –15 V	0.1 (1)		0.3	
P_O	Output power					6	W
V_I	Input voltage range	Over I_O range		2.9		7	V
V_O	Set-point voltage tolerance	T_A = 25°C			±3 (3)		%
	Temperature variation	–40°C to +85°C			±0.5		$\%V_O$
	Line regulation	Over V_I range			0.5		$\%V_O$
	Load regulation	Over I_O range			0.25		$\%V_O$
	Total output voltage variation	Includes set point, line, load –40 < T_A < 85°C			±5 (3)		$\%V_O$
V_O Adj	Output voltage adjust range			–15		–3.3	V
η	Efficiency	R_{SET} = 523 Ω, V_O = –15 V, I_O = 0.3 A			80		%
		R_{SET} = 1.96 kΩ, V_O = –12 V, I_O = 0.5 A			82		
		R_{SET} = 4.53 kΩ, V_O = –9 V, I_O = 0.6 A			83		
		R_{SET} = 15.4 kΩ, V_O = –5 V, I_O = 1.0 A			82		
		R_{SET} = 36.5 kΩ, V_O = –3.3 V, I_O = 1.0 A			78		
V_r	Output voltage ripple	20-MHz bandwidth			3% V_O		$V_{(PP)}$
$I_{O\ (LIM)}$	Current limit threshold	Reset, followed by auto-recovery			150		$\%I_{Omax}$
	Transient response	1 A/µs load step from 50% to 100% $I_O$max (4)	Recovery time		100		µs
			V_O over/undershoot		2		$\%V_O$
F_S	Switching frequency	Over V_I and I_O ranges		210	260	310	kHz
UVLO	Undervoltage lockout	V_I increasing			2.50	2.55	V
		V_I decreasing		2.30	2.40		
	Inhibit control (pin 3)	Input high voltage (V_{IH})		V_I – 0.5		Open (5)	V
		Input low voltage (V_{IL})		–0.2		+0.25	
		Input low current (I_{IL})			10		µA
I_I inh	Inhibit standby current	Inhibit (pin 3) to GND (pin 1)			470		µA
C_I	External input capacitance			100 (6)			µF
C_O	External output capacitance	Ceramic		0		100 (7)	µF
		Nonceramic		100 (8)		560 (9)	µF
		Equivalent series resistance (nonceramic)		10 (10)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		7.5			10^6 Hrs

(1) The module will operate down to no load with reduced specifications.
(2) The maximum output current is 1 A or the maximum output power is 6 W, whichever is less.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(4) A load step from 66% to 100% $I_O$max for V_O = –15 V.
(5) This control pin has an internal pull-up to the input voltage, V_I. If it is left open circuit, the module operates when input power is applied. A small, low-leakage (< 100 nA) metal-oxide semiconductor field effect transistor (MOSFET) is recommended for control. See the application Information for further guidance.
(6) 100 µF of capacitance is required across the input (V_I and GND) for proper operation. Locate the ceramic capacitance close to the module.
(7) When using ceramic output capacitance equivalent to 100 µF, a 100 µF electrolytic capacitor is also required.
(8) 100 µF of output capacitance is required for proper operation. See the application information for further guidance.
(9) The minimum ESR limitation may result in a lower value for the output capacitance. See the Input/Output Capacitor Recommendations for further guidance.
(10) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using maximum ESR values to calculate.

PIN ASSIGNMENT

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1		The common ground connection for the V_I and V_O power connections. It is also the reference for the V_O *Adjust* control inputs.
V_I	2	I	The positive input voltage power node to the module, which is referenced to common GND.
Inhibit	3	I	The Inhibit pin is an open-collector/drain (non-TTL), negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output. When the Inhibit control is active-low, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output voltage whenever a valid input source is applied. The PTN04050A Inhibit control circuitry must not be shared with another module. Never connect a resistor between the Inhibit pin and any other voltage reference or GND.
V_O Adjust	4	I	A 1% resistor must be connected between pin 4 and pin 1 to set the output voltage of the module. If left open-circuit, the output voltage defaults to –1.79 V, which is beyond the recommended operating range. The set-point range is –15 V to –3.3 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The standard resistor value for a number of common output voltages is provided in the application information.
V_O	5	O	The negative output voltage power node with respect to the GND node.



TYPICAL CHARACTERISTICS (3.3-V INPUT)(1)(2)

EFFICIENCY VS OUTPUT CURRENT

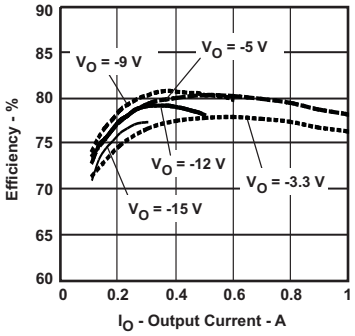


Figure 1.

OUTPUT VOLTAGE RIPPLE VS OUTPUT CURRENT

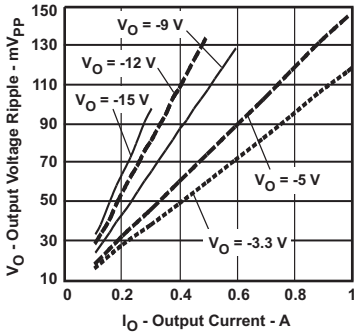


Figure 2.

POWER DISSIPATION VS OUTPUT CURRENT

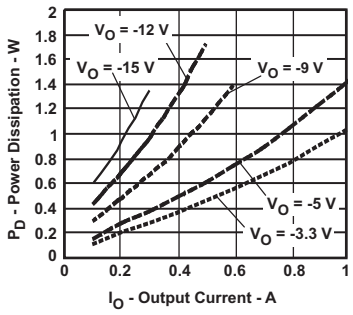


Figure 3.

TEMPERATURE DERATING VS OUTPUT CURRENT

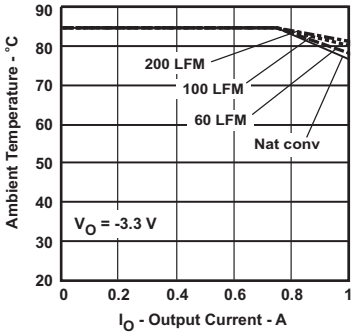


Figure 4.

TEMPERATURE DERATING VS OUTPUT CURRENT

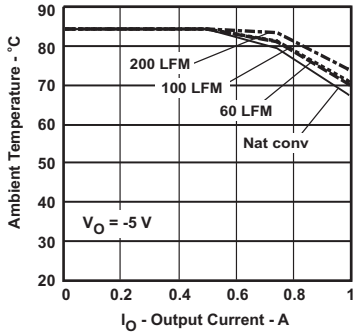


Figure 5.

TEMPERATURE DERATING VS OUTPUT CURRENT

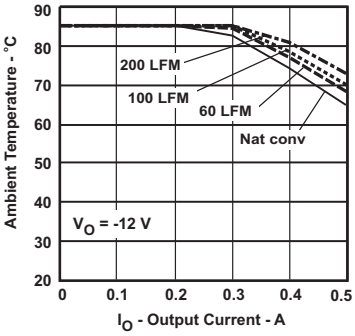


Figure 6.

TEMPERATURE DERATING VS OUTPUT CURRENT

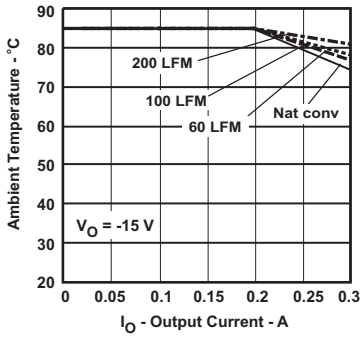


Figure 7.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. Applies to Figure 4, Figure 5, Figure 6, and Figure 7.

TYPICAL CHARACTERISTICS (5-V INPUT)(1)(2)

EFFICIENCY VS OUTPUT CURRENT

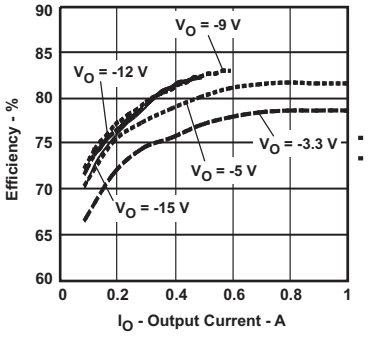


Figure 8.

OUTPUT VOLTAGE RIPPLE VS OUTPUT CURRENT

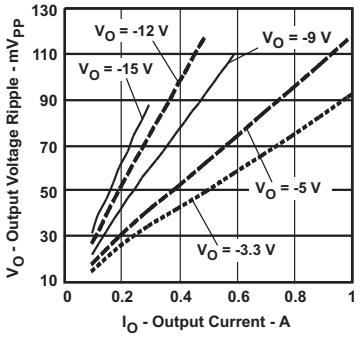


Figure 9.

POWER DISSIPATION VS OUTPUT CURRENT

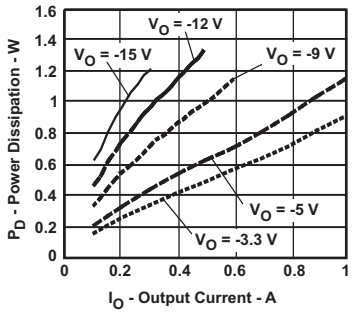


Figure 10.

TEMPERATURE DERATING VS OUTPUT CURRENT

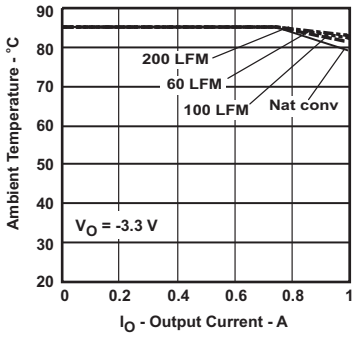


Figure 11.

TEMPERATURE DERATING VS OUTPUT CURRENT

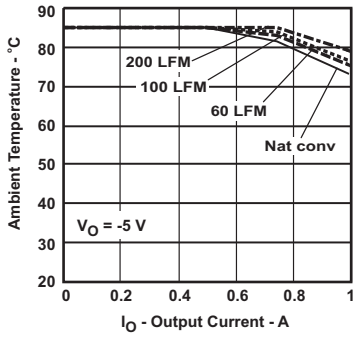


Figure 12.

TEMPERATURE DERATING VS OUTPUT CURRENT

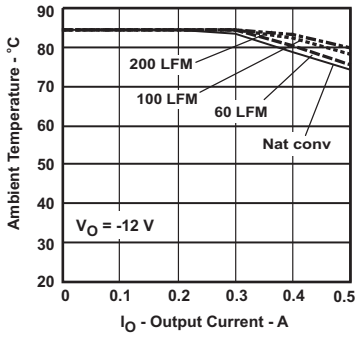


Figure 13.

TEMPERATURE DERATING VS OUTPUT CURRENT

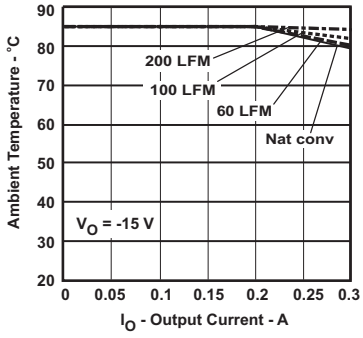


Figure 14.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 8, Figure 9, and Figure 10.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100-mm x 100-mm, double-sided PCB with 2 oz. copper. Applies to Figure 11, Figure 12, Figure 13, and Figure 14.

APPLICATION INFORMATION

Adjusting the Output Voltage of the PTN04050A Wide-Output Adjust Power Modules

General

A resistor must be connected directly between the *V_O Adjust* control (pin 4) and GND (pin 1) to set the output voltage of the module. The adjustment range is from –15 V to –3.3 V. If pin 4 is left open, the output voltage defaults to –1.79 V, which is beyond the recommended operating range.

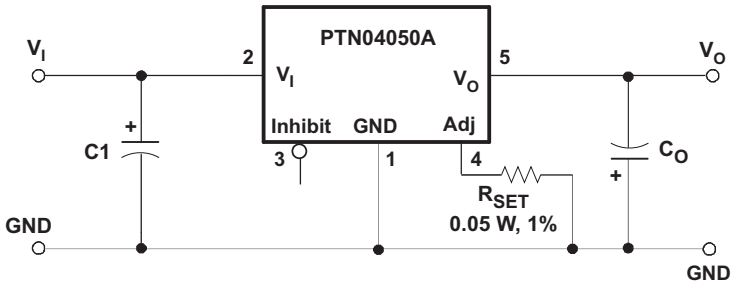
Table 1 gives the standard resistor value for a number of common voltages, along with the actual output voltage that the value produces. For other output voltages, the resistor value can either be calculated using Equation 1, or by selecting from the range of values given in Table 2. Figure 15 shows the placement of the required resistor.

$$R_{SET} = -4.34\ k\Omega \times \frac{V_O + 16.6\ V}{V_O + 1.734\ V} \quad (1)$$

Table 1. Standard Values of R_{set} for Common Output Voltages

V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)
–15 V (1)	523 Ω	–15.00 V
–12 V (2)	1.91 kΩ	–12.02 V
–5 V (2)	15.4 kΩ	–5.00 V
–3.3 V (2)	36.5 kΩ	–3.31 V

(1) For V_O = –12.6 V to –15 V the maximum output current is limited to 0.3 A.
(2) For V_O = –3.3 V to – 12.6 V the maximum output current is 1 A or the maximum output power is 6 W, whichever is less.



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close as possible to the regulator. Connect the resistor directly between pins 4 and 1 using dedicated PCB traces.

(2) Never connect capacitors from *V_O Adjust* to either *GND* or *V_O*. Any capacitance added to the *V_O Adjust* pin affects the stability of the regulator.

Figure 15. V_O Adjust Resistor Placement

Table 2. Output Voltage Set-Point Resistor Values

V_O Required	R_{SET}	V_O Required	R_{SET}	V_O Required	R_{SET}
–15.0 V	523 Ω	–11.9 V	2.00 kΩ	–8.8 V	4.75 kΩ
–14.9 V	562 Ω	–11.8 V	2.05 kΩ	–8.6 V	5.11 kΩ
–14.8 V	604 Ω	–11.7 V	2.15 kΩ	–8.4 V	5.36 kΩ
–14.7 V	634 Ω	–11.6 V	2.21 kΩ	–8.2 V	5.62 kΩ
–14.6 V	681 Ω	–11.5 V	2.26 kΩ	–8.0 V	5.90 kΩ
–14.5 V	715 Ω	–11.4 V	2.32 kΩ	–7.8 V	6.34 kΩ
–14.4 V	750 Ω	–11.3 V	2.37 kΩ	–7.6 V	6.65 kΩ
–14.3 V	787 Ω	–11.2 V	2.49 kΩ	–7.4 V	7.15 kΩ
–14.2 V	845 Ω	–11.1 V	2.55 kΩ	–7.2 V	7.50 kΩ
–14.1 V	887 Ω	–11.0 V	2.61 kΩ	–7.0 V	7.87 kΩ
–14.0 V	931 Ω	–10.9 V	2.67 kΩ	–6.8 V	8.45 kΩ
–13.9 V	953 Ω	–10.8 V	2.80 kΩ	–6.6 V	8.87 kΩ
–13.8 V	1.00 kΩ	–10.7 V	2.87 kΩ	–6.4 V	9.53 kΩ
–13.7 V	1.05 kΩ	–10.6 V	2.94 kΩ	–6.2 V	10.2 kΩ
–13.6 V	1.10 kΩ	–10.5 V	3.01 kΩ	–6.0 V	10.7 kΩ
–13.5 V	1.15 kΩ	–10.4 V	3.09 kΩ	–5.8 V	11.5 kΩ
–13.4 V	1.18 kΩ	–10.3 V	3.16 kΩ	–5.6 V	12.4 kΩ
–13.3 V	1.24 kΩ	–10.2 V	3.32 kΩ	–5.4 V	13.3 kΩ
–13.2 V	1.30 kΩ	–10.1 V	3.40 kΩ	–5.2 V	14.3 kΩ
–13.1 V	1.33 kΩ	–10.0 V	3.48 kΩ	–5.0 V	15.4 kΩ
–13.0 V	1.40 kΩ	–9.9 V	3.57 kΩ	–4.8 V	16.5 kΩ
–12.9 V	1.43 kΩ	–9.8 V	3.65 kΩ	–4.6 V	18.2 kΩ
–12.8 V	1.50 kΩ	–9.7 V	3.74 kΩ	–4.4 V	19.6 kΩ
–12.7 V	1.54 kΩ	–9.6 V	3.83 kΩ	–4.2 V	21.5 kΩ
–12.6 V	1.58 kΩ	–9.5 V	3.92 kΩ	–4.0 V	24.3 kΩ
–12.5 V	1.65 kΩ	–9.4 V	4.12 kΩ	–3.8 V	26.7 kΩ
–12.4 V	1.69 kΩ	–9.3 V	4.22 kΩ	–3.6 V	30.1 kΩ
–12.3 V	1.78 kΩ	–9.2 V	4.32 kΩ	–3.4 V	34.0 kΩ
–12.2 V	1.82 kΩ	–9.1 V	4.42 kΩ	–3.3 V	37.4 kΩ
–12.1 V	1.87 kΩ	–9.0 V	4.53 kΩ		
–12.0 V	1.96 kΩ	–8.9 V	4.64 kΩ		

CAPACITOR RECOMMENDATIONS FOR THE PTN04050A NEGATIVE-OUTPUT ADJUST POWER MODULES

Input Capacitor

The minimum requirement for the input bus is 100 µF of capacitance. The minimum ripple current rating for any nonceramic capacitance must be at least 250 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input. This ripple current requirement can be reduced by placing ceramic capacitors at the input.

If tantalum capacitors are used at the input bus, a minimum voltage rating of 2 × (maximum dc voltage + ac ripple) is standard practice to ensure reliability. Polymer-tantalum capacitors are more reliable and are available with a maximum rating of typically 20 V.

Output Capacitor

The minimum capacitance required to ensure stability is a 100 µF. Either ceramic or electrolytic-type capacitors can be used. The minimum ripple current rating for the nonceramic capacitance must be at least 200 mA rms. The stability of the module and voltage tolerances is compromised if the capacitor is not placed near the output bus pins. A high-quality, computer-grade electrolytic capacitor should be adequate. When using ceramic capacitance equivalent to 100 µF, a 100 µF electrolytic is also required.

For applications with load transients (sudden changes in load current), the regulator response improves with additional capacitance. Additional electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or Os-Con-type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 mΩ (17 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of recommended capacitors and vendors are identified in Table 3.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further reduce the reflected input ripple current, or the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR, and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 200 µF.

Tantalum Capacitors

Tantalum-type capacitors may be used at both the input and the output, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

The capacitor table, Table 3, identifies the characteristics of capacitors from various vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation of any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

Table 3. Recommended Input/Output Capacitors

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (I_{rms}) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Panasonic FC(Radial)	25	180	0.117	555	8 X 11	1	1	EEUFC1E181
Panasonic FC (SMD)	25	100	0.30	450	8 X 10,2	1	1	EEVFC1E101P
United Chemi-Con PXA (SMD)	16	150	0.026	3430	10 X 7,7	1	1	PXA16VC151MJ80TP (V_O≤ 13 V)
PS	25	100	0.020	4320	10 X 12,5	1	1	25PS100MJ12
LXZ	25	100	0.250	290	6,3 X 11,5	1	1	LXZ25VB101M6X11LL
MVY(SMD)	35	100	0.300	450	8 X 10	1	1	MVY35VC101MH10TP
Nichicon UWG (SMD)	50	100	0.300	500	10 X 10	1	1	UWG1H101MNR1GS
F559 (Tantalum)	10	100	0.055	2000	7,7 X 4,3	1	1 (1)	F551A107MN (V_O≤ 5 V)
HD	25	100	0.130	405	6,3 X 11	1	1	UHD1E101MER
Sanyo Os-Con SVP (SMD)	20	100	0.024	2500	8 X 12	1	1	20SVP100M
SP	16	100	0.032	2890	10 X 5	1	1 (1)	16SP100M (V_O≤ 14 V)
AVX Tantalum TPS (SMD)	20	100	0.085	1543	7,3L X 4,3W X 4,1H	1	≤1 (1)	TPSV107M020R0085 (V_O≤ 10 V)
	20	100	0.200	> 817		1	≤1 (1)	TPSE107M020R0200 (V_O≤ 10 V)
Murata X5R Ceramic	6.3	100	0.002	>1000	3225	1	≤1 (1)	GRM32ER60J107M (V_O≤ 5.5 V)
TDK X5R Ceramic	6.3	100	0.002	>1000	3225	1	≤1 (1)	C3225X5R0J107MT (V_O≤ 5.5 V)
Murata X5R Ceramic	16	47	0.002	>1000	3225	2	≤2 (1)	GRM32ER61C476M (V_o≤ 13.5 V)
Kemet X5R Ceramic	6.3	47	0.002	>1000	3225	2	≤2 (1)	C1210C476K9PAC (V_O≤ 5.5 V)
TDK X5R Ceramic	6.3	47	0.002	>1000	3225	2	≤2 (1)	C3225X5R0J476MT (V_O≤ 5.5 V)
Murata X5R Ceramic	6.3	47	0.002	>1000	3225	2	≤2 (1)	GRM422X5R476M6.3 (V_O≤ 5.5 V)
TDK X5R Ceramic	16	22	0.002	>1000	3225	5	≤5 (1)	C3225X5R1E2265KT/MT (V_O≤ 14 V)
Murata X7R Ceramic	25	22	0.002	>1000	3225	5	≤5	GRM32ER61C226K
Kemet X7R Ceramic	16	22	0.002	>1000	3225	5	≤5 (1)	C1210C226K3PAC (V_O≤ 14 V)

(1) The maximum voltage rating of the capacitor must be selected for the desired set-point voltage (V_O). To operate at a higher output voltage, select a capacitor with a higher voltage rating.

Power-Up Characteristics

When configured per the standard application, the PTN04050A power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a time delay (typically 60 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 16 shows the power-up waveforms for a PTN04050A, operating from a 5-V input and with the output voltage adjusted to –12 V. The waveforms were measured with a 500-mA resistive load.

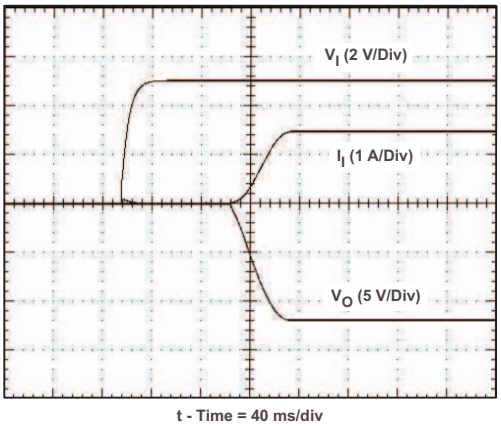


Figure 16. Power-Up Waveforms

Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the module from attempting to power up until the input voltage is above the UVLO threshold. This prevents the module from drawing excessive current from the input source at power up. Below the UVLO threshold, the module is held off.

Current Limit Protection

The PTN04050 modules protect against load faults with a continuous current limit characteristic. Under a load fault condition, the output current cannot exceed the current limit value. Attempting to draw current that exceeds the current limit value causes the module to progressively reduce its output voltage. Current is continuously supplied to the fault until it is removed. On removal of the fault, the output voltage promptly recovers. When limiting output current, the regulator experiences higher power dissipation, which increases its temperature. If the temperature increase is excessive, the module's overtemperature protection begins to periodically turn the output voltage completely off.

Overtemperature Protection

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current-limit condition. If the junction temperature of the internal control IC rises excessively, the module turns itself off, reducing the output voltage to zero. The module instantly restarts when the sensed temperature decreases by a few degrees.

Note: *Overtemperature protection is a last-resort mechanism to prevent damage to the module. It should not be relied on as permanent protection against thermal stress. Always operate the module within its temperature derated limits, for the worst-case operating conditions of output current, ambient temperature, and airflow. Operating the module above these limits, albeit below the thermal shutdown temperature, reduces the long-term reliability of the module.*

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTN04050A power module incorporates an output on/off Inhibit control (pin 3). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 17 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pullup to V_I. An open-collector or open-drain (non-TTL) device is required to control this input.

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. Figure 18 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 500-mA resistive load.

Note: *The PTN04050A Inhibit control circuitry must not be shared with another module. Never connect a resistor between the Inhibit pin and any voltage reference or GND.*

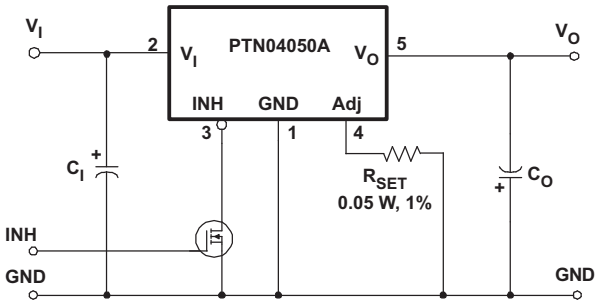


Figure 17. Inhibit Circuit

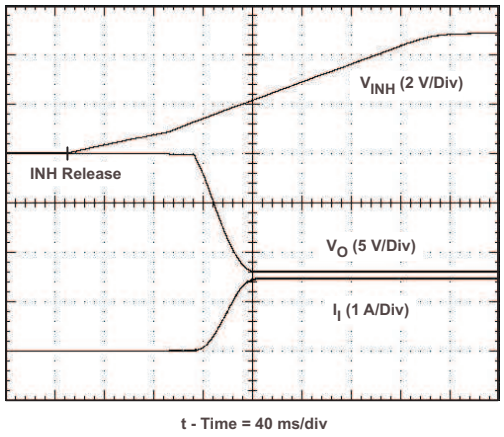


Figure 18. Inhibit Waveform

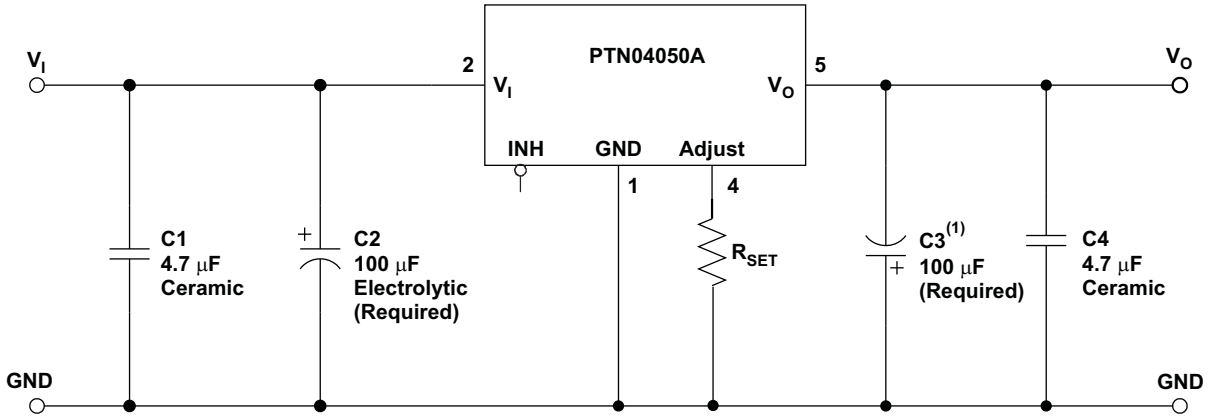
Optional Input/Output Filters

Power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

Input/Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more 4.7-µF ceramic capacitors, such as C4 shown in Figure 19. Ceramic capacitors should be placed close to the output power terminals. A single 4.7-µF capacitor reduces the output ripple/noise by 10% to 30%. (Note: C3 is required to improve the regulators transient response and does not reduce output ripple and noise.)

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of C1, minimum 4.7-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by 20% to 30%.



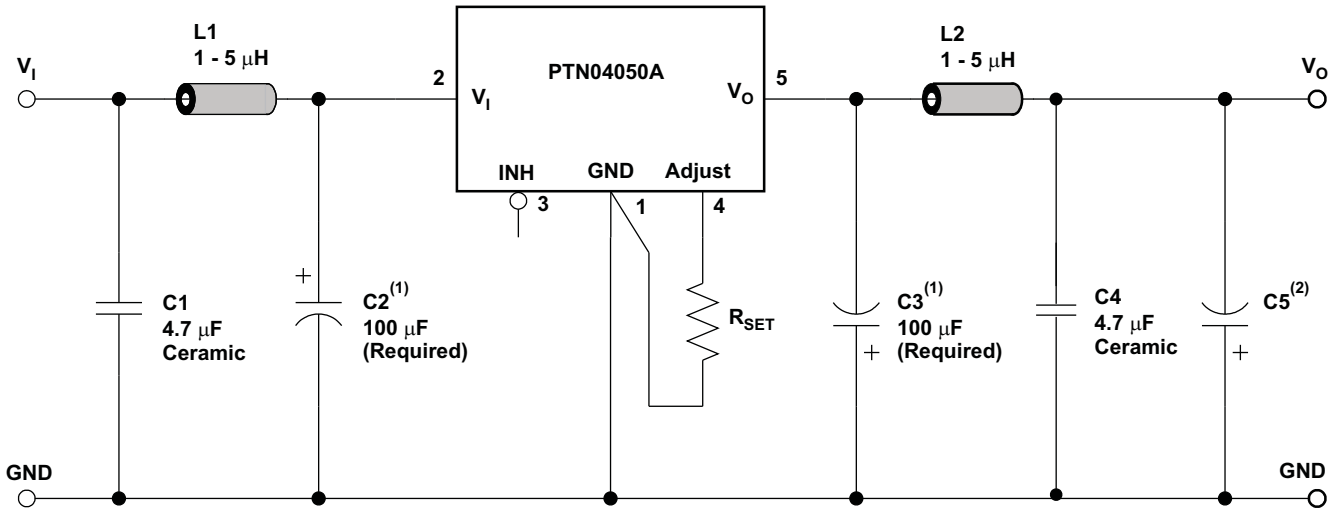
(1) See Table 3 for suggested value and type.

Figure 19. Adding High-Frequency Bypass Capacitors to the Input and Output

π Filters

If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead (Fair-Rite Pt. No. 2673000701 or equivalent) in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 20 and Figure 21). In order for the inductor to be effective in reduction of ripple and noise ceramic capacitors are required. (See the Capacitor Recommendations for the PTN04050A for additional information on vendors and component suggestions.)

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency (650 kHz - 1 MHz). The placement of this filter is critical. It must be located as close as possible to the input or output pins to be effective. The ferrite bead is small (12,5 mm × 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite also manufactures a surface-mount bead (part number 2773021447), through hole (part number 2673000701) rated to 5 A. Alternatively, 1-µH to 5-µH inductors can be used in place of the ferrite inductor bead.



(1) See Table 3 for suggested value and type.

(2) Recommended for application with load transients.

Figure 20. Adding π Filters

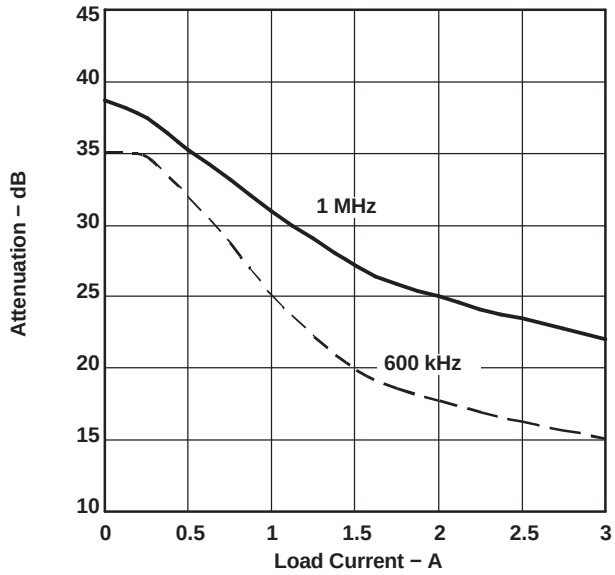


Figure 21. π-Filter Attenuation vs. Load Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTN04050AAH	OBSOLETE	Through-Hole Module	EUU	5		RoHS (In Work) & Green (In Work)			-40 to 85		
PTN04050AAS	OBSOLETE	Surface Mount Module	EUV	5		Non-RoHS & Green (In Work)			-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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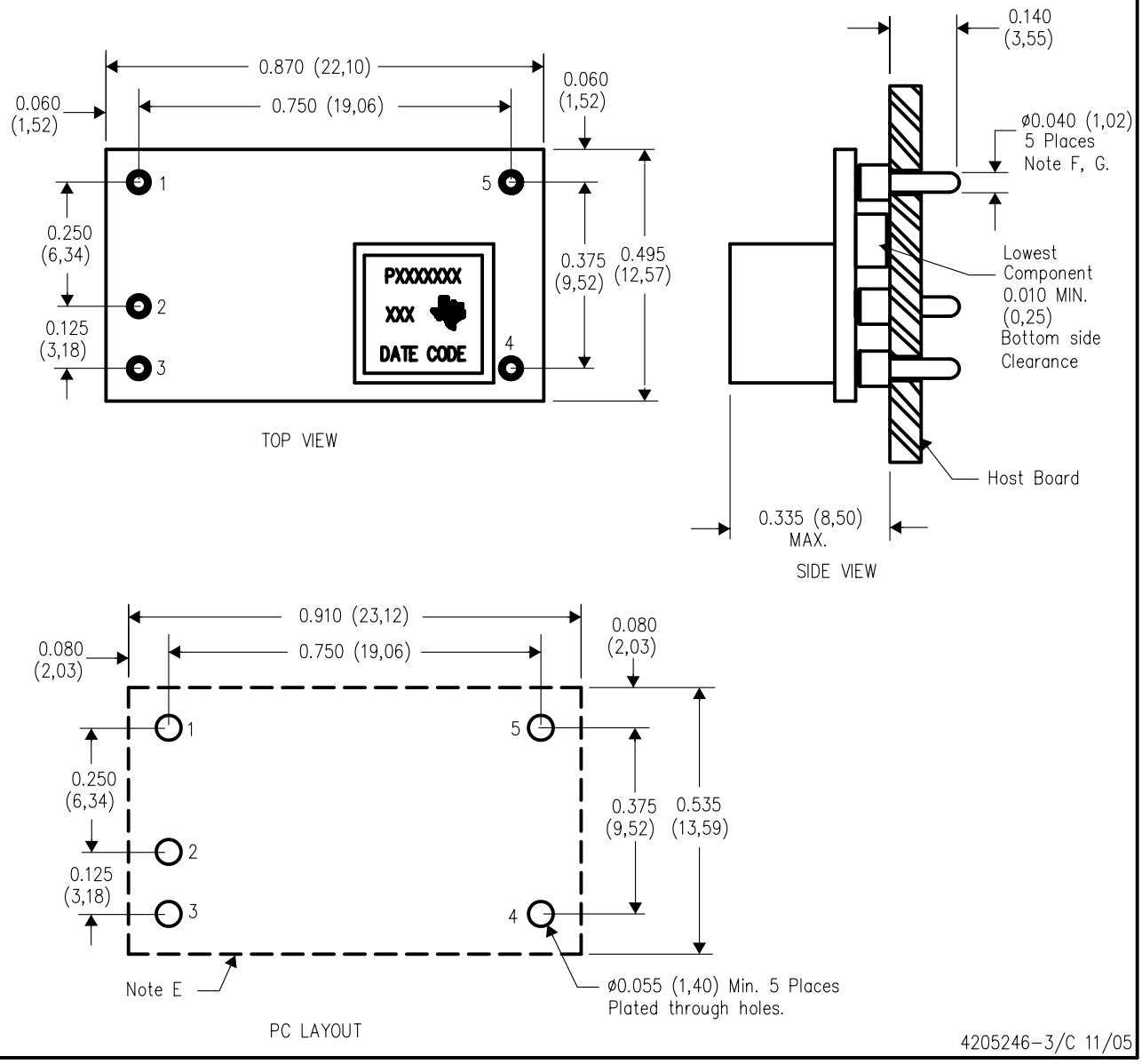
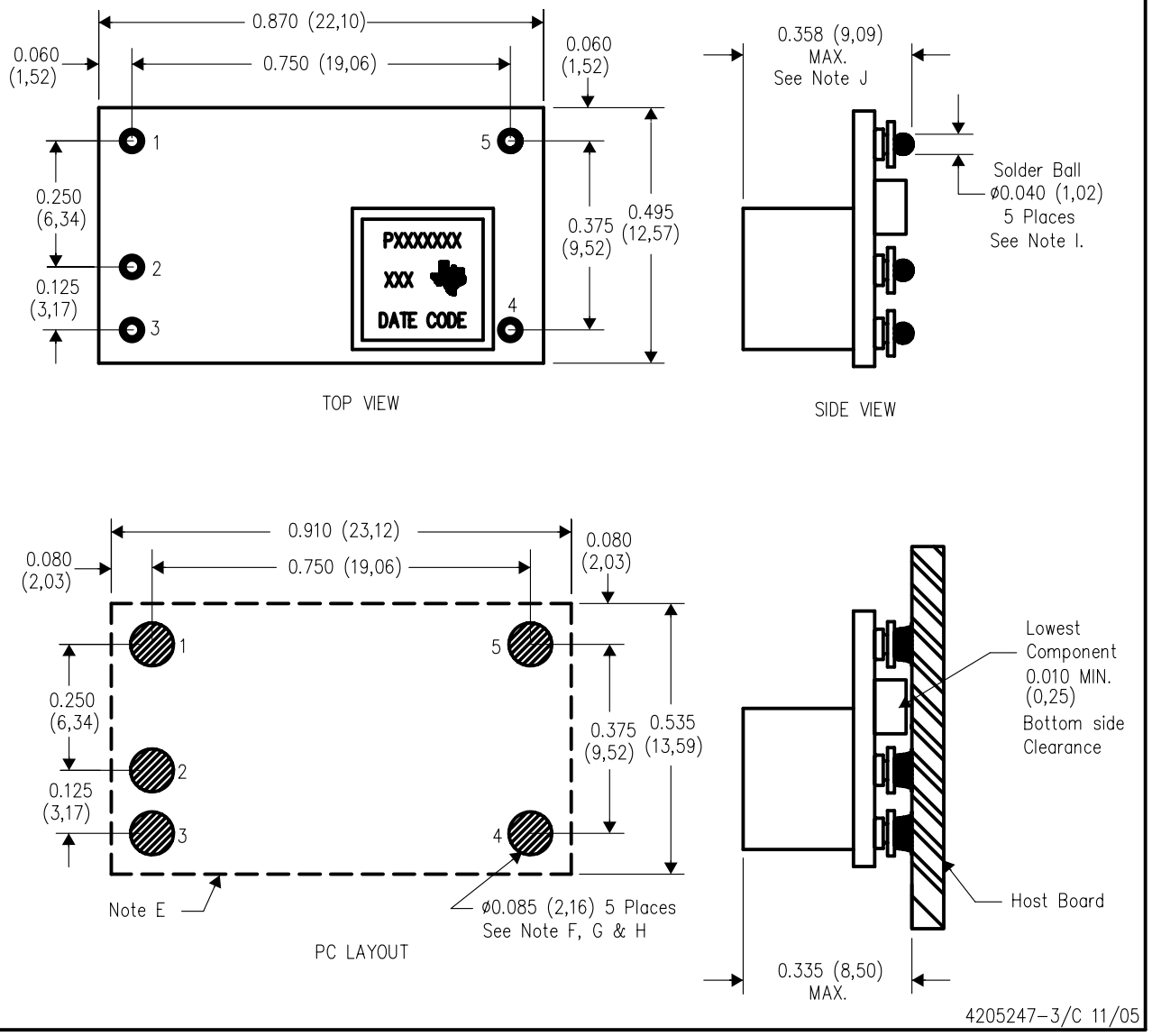
EUU (R–PDSS–T5) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUV (R–PDSS–B5) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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